

Atomically-thin Half van der Waals Metals, Alloys and Compounds Stabilized via Confinement Heteroepitaxy

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Abstract: Two dimensional (2D) monoelemental metals, alloys, and compounds exhibit various unique structural, optical, transport, and quantum phenomena due to their reduced dimensionality, underscoring their potentially critical role in next-generation quantum technologies. Yet, until recently, the synthesis of large-area continuous sheets of 2D metals, alloys, and compounds for device integration beyond traditional van der Waals materials has posed a significant challenge due to oxidation of the material in ambient conditions. To answer this, we have leveraged previous work on modulating epitaxial graphene (EG) via intercalation to develop a unique synthesis route dubbed confinement heteroepitaxy (CHet). In the CHet method, intercalation of an atomic species within a high energy interface between EG and silicon carbide (SiC (0001)) creates environmentally stable, crystalline, atomically thick metals (Ga, In, Ag, Pb, Au, etc.), alloys (InGa, and PbGa) and compounds (Ga₂O₃, GaN, InN, etc.) epitaxial to the SiC substrate. The composition of the 2D intercalant is controlled by altering the metallic precursor that is evaporated onto the EG surface or by post-processing, e.g. oxidation and nitridation. We demonstrate that CHet-based 2D materials exhibit divergent properties from the bulk, including a 4x increase in the superconducting transition temperature, metallic to semiconducting transition, extraordinary nonlinear susceptibility (χ^2) values above 10 nm/V, and a large spin orbital coupling gap nearing 500 meV, transition from anti-ferromagnetism to ferromagnetism. Furthermore, 2D non-layered semiconductors, such as 2D Ga₂O₃, exhibit a bandgap significantly larger than their bulk counterparts (6.6 eV in 2D vs. 4.8 eV in bulk r-Ga₂O₃). We also show that they remain intact after ex-situ post-processing and post-treatment (such as lithography), implicating facile integration as metasurfaces, tunnelling barriers, substrates, and device platforms.