Three-dimensional integration of two-dimensional field-effect transistors

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Project summary: With the escalating costs of developing and manufacturing integrated circuit (IC) chips, methods to vertically stack devices are being thoroughly explored. While silicon-based 3D ICs have been achieved using innovative packaging solutions, there has been limited exploration of emerging nanomaterials, such as 2D Transition metal dichalcogenides (TMDs), for a monolithic 3D chip. In this study, we showcase the following achievements: (1) wafer-scale two-tier 3D integration based on MoS_2, with each tier containing over 10,000 field-effect transistors (FETs); (2) three-tier chip using both MoS_2 and WSe_2, with 500 FETs in each tier; and (3) two-tier chip featuring 200 scaled MoS_2 FETs of channel length L_{CH} = 45 nm in each tier. Additionally, we show the multifunctionality of 2D materials by demonstrating a vertically connected 3D circuit, along with sensing and storage capabilities. This demonstration not only paves the way for the development of functionally divergent ICs, but also highlights the potential for 2D materials for 3D integrated chips.

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2DCC Role: Wafer-scale MoS_2 and WSe_2 monolayers grown by MOCVD in the 2DCC-MIP facility were used in the study.