Doping Strategy to achieve High-performance p-type Two-dimensional Field Effect Transistors

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The rise of atomically thin 2D semiconductors, such as MoS₂ and WSe₂, marks a profound departure from conventional silicon-based CMOS technology. While substantial progress has been made in advancing n-type Field-Effect Transistors (FETs) based on these materials to meet the rigorous standards set by the International Roadmap for Devices and Systems (IRDS), persistent challenges hinder the realization of high-performance p-type FETs. Chief among these challenges is Fermi level pinning at metal/2D interfaces, which poses a formidable barrier to achieving optimal device performance. In materials like MoS₂ and WS₂, the use of low work-function metals presents a promising avenue for enhancing n-type FETs. However, this approach exacerbates contact resistance for hole injection, impeding the efficient operation of p-type FETs. Conversely, transition metal selenides like MoSe₂ and WSe₂ offer improved hole injection characteristics due to Fermi level pinning. Nonetheless, the trade-off comes in the form of reduced ON-state performance, attributed to tunneling across the Schottky barrier.

Addressing these multifaceted challenges demands innovative strategies, particularly in the domain of degenerate doping beneath contacts, a critical yet intricate aspect of 2D FET design. Through a comprehensive examination of 2D FETs based on both pristine and doped MoSe₂ and WSe₂ flakes, researchers have uncovered intriguing insights. Pristine flakes exhibit dominant n-type transport, whereas thicker doped flakes demonstrate enhanced degenerate p-type doping. However, the thicker flakes suffer from compromised electrostatic gate control, resulting in a suboptimal on/off current ratio. Conversely, reducing flake thickness leads to diminished doping effectiveness, owing to quantum confinement effects.

In response to these findings, a novel FET architecture has been proposed, integrating thin channel layers with degenerately doped multilayer contact regions. This innovative design represents a paradigm shift in 2D FET engineering and has yielded remarkable performance characteristics. The proposed FET structure showcases an impressive ON-current of approximately 85μ A/µm, coupled with low RC (~2 k Ω -µm), indicative of efficient carrier transport. Furthermore, the device boasts a remarkable ON/OFF current ratio of 10^4 , underscoring its efficacy in switching between states. Moreover, the integration of dual gate architecture and aggressive scaling with the proposed FET structure has further amplified its performance metrics. Through meticulous optimization and experimental validation, an unprecedented ON-state current density of approximately 212µA/µm has been achieved. This notable enhancement underscores the versatility and scalability of the

proposed FET architecture, suggesting its potential for widespread adoption in advancing 2D FET technology.