Monolithic and heterogeneous three-dimensional (3D) integration of two-dimensional (2D) materials using dense vias

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Abstract: The semiconductor industry is experiencing a tectonic shift with the adoption of three-dimensional (3D) integration, enabling the convergence of various technologies, such as analogue, radio frequency, sensors, memory devices, and digital components. Historically, through-silicon via (TSV) stacking has been the dominant approach to 3D integration, leading to the commercialization of 3D-stacked CMOS image sensors, 3D flash memories, and dynamic random-access memory (DRAM) stacks. While TSV technology can achieve impressive interconnect (I/O) densities of up to 10,000 I/O per mm^2, further improvement requires the adoption of monolithic 3D integration (M3D). M3D also enables transistor-level partitioning and material heterogeneity. However, widespread use of non-silicon materials in M3D is pending. In this study, we showcase heterogeneous M3D integration using all-two-dimensional (all-2D) materials, achieving an interconnect density of 40,000 I/O per mm^2 with more than 500 devices in each tier. Additionally, our manufacturing process stays below 200°C, which is ideal for back-end-of-line (BEOL) integration. The M3D stack in our study includes graphene-based chemisensors in tier 2 and MoS_2 memtransistor-based programmable circuits in tier 1, tailored for near-sensor computing applications. A notable achievement in our work is the physical proximity between sensors and computing elements, which is less than 100 nm. This proximity far surpasses what is currently achievable with state-of-the-art packaging solutions. Our results mark a significant milestone in vertically stacked functional layers composed of heterogeneous materials beyond silicon for edge applications.