Modeling and Characterization of Gate-All-Around Vertical Nanowire Array Transistors Based on Van Der Waals Epitaxial InAs-on-2D Heterostructures

John Wyatt Morrell[a,b], Muhammad Shaffatul Islam,[c,d] Alireza Abrand[c,d], Nithil Harris Manimaran[d], Parsian K. Mohseni[b,c,d,e], Ke Xu[a,b,d]

[a]Physics & Astronomy, [b]Chemistry & Materials Science, [c]Nanopower Research Laboratories, [d]Microsystems Engineering, [e]Electrical & Microelectronic Engineering, Rochester Institute of Technology.

III-V semiconductors show promise as channel materials in next generation nanoelectronics.[1,2] Among III-V materials, InAs stands out as a potential replacement for n-type channel material in complimentary metal-oxide-semiconductor (CMOS) based devices.[3,4] Compared with silicon, InAs offers 30 times the electron mobility and a higher ON current, and when grown as a 1D InAs nanowire (NW), this mobility is further enhanced compared to thin-film and bulk InAs.[3] For NW based transistors, a gate-all-around (GAA) geometry offers better electrostatic gating but proves to bemore difficult in fabrication process, especially with vertical NWs.[3] In order to solve this issue, electric double layer (EDL) gating can be used. EDL gating is a method which uses an electric field to control mobile ions within an electrolyte to create strong local electric fields. Due to the accumulation of ions in the electrolyte ~1 nm from the channel, fields on the order of 10 MV/cm can be achieved, allowing for high carrier density in semiconducting materials (including 2D and III-V materials)[5]. Additionally, the strength of EDL gating is weakly dependent on gate to channel distance, which allows for flexibility in device geometry without sacrificing carrier density. EDL gating can support otherwise difficult to fabricate geometries such as vertical GAA NW FETs. In this study, we first simulate the operation and performance of electrolyte-gated junctionless III-V nanowire (NW) transistors composed of compositionally-graded InGaAs channels. Modeling results indicated two orders of magnitude improvement in I_{on}/I_{off} ratio and ~30 mV/dec reduction in subthreshold slope compared to conventional junctionless oxide-gated NW transistors, demonstrating that EDL gating provides improved electrostatic integrity. Experimentally, the NW transistors were fabricated with vertical InAs NWs epitaxially grown on graphene, with solid electrolyte permeating between NWs, topped with a metal electrode contacting the top of the NWs. I will discuss device fabrication process and initial electrical characterizations, and plans for further materials characterization via Raman, SEM, and AFM.

1. R, Ullah, et al, *Physical Review Materials* 2.2 (2018), 025601.
2. Barrigón, Enrique, et al, *Chemical Reviews* 119.15 (2019) , 9170-9220.
3. Zhang, Chen, et al, *IEEE Transactions on Electron Devices* 63.1 (2016), 223-234.
4. Lieb, Johanna , et al, *Advanced Functional Materials* 29.3 (2019), 1804378.
5. Xu, Ke and Fullerton, Susan, *J. Phys. Mater* 3.3 (2020) 032001.