

Monolithic Three-Dimensional Integration of Two-Dimensional Field Effect Transistors

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The semiconductor industry is evolving from “Moore's Law” to the "More Moore" era, propelled by three-dimensional (3D) integration that transcends the limitations of conventional two-dimensional (2D) scaling. This pioneering method elevates device integration density, performance, energy efficiency, and the overall functionality of integrated circuits (ICs). While innovative packaging solutions have made 3D integrated circuits commercially viable, the inclusion of through-silicon vias (TSVs) and microbumps brings about significant area overhead and introduces parasitic capacitances that limit overall performance. Monolithic 3D integration (M3D) is regarded as the future of 3D ICs, yet its application faces hurdles in silicon ICs due to restricted thermal processing budgets in upper tiers, which can degrade device performance. To overcome these limitations, emerging materials like carbon nanotubes (CNTs) and 2D semiconductors have been integrated into the back end of silicon ICs, albeit with the added complexity of heterogeneous integration. Here we demonstrate, 1) wafer-scale and monolithic 2-tier 3D integration based on MoS₂ with more than 10000 field-effect transistors (FETs) in each tier, 2) 3-tier 3D integration based on both MoS₂ and WSe₂ with ~500 FETs in each tier, and 3) 2-tier 3D integration based on 200 scaled MoS₂ FETs (channel length, $L_{CH} = 45$ nm) 4) integration of complementary WSe₂ FETs, in which the n-type FETs are placed in tier 1 and the p-type FETs are placed in tier 2. 5) achieved dense and scaled integration through 300 nm vias with pitch < 1 μ m connecting more than 300 devices in tier 1 and 2. Moreover, we have effectively implemented vertically integrated logic gates, encompassing inverters, NAND gates, and NOR gates. Our demonstration emphasizes the significance of 2D materials in expediting the M3D integration of CMOS circuits, driving forward the "More Moore" era.